9621
DUAL-LINE DRIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

FEATURES

- **CCSL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

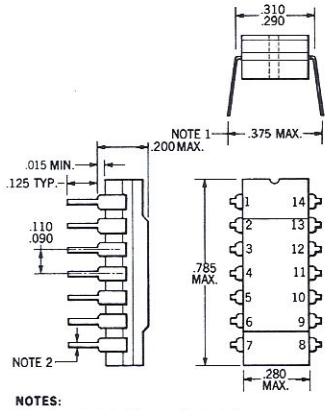
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−.5 V to +15 V
Voltage Applied to Outputs	−2 V to +V_{CC1} + 1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ORDER INFORMATION

Specify U6A9621XXX for 14 pin Dual In-Line Package or U319621XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

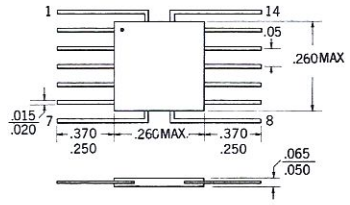
TYPICAL DUAL IN-LINE PACKAGE

Similar to
JEDEC (TO-116) Outline

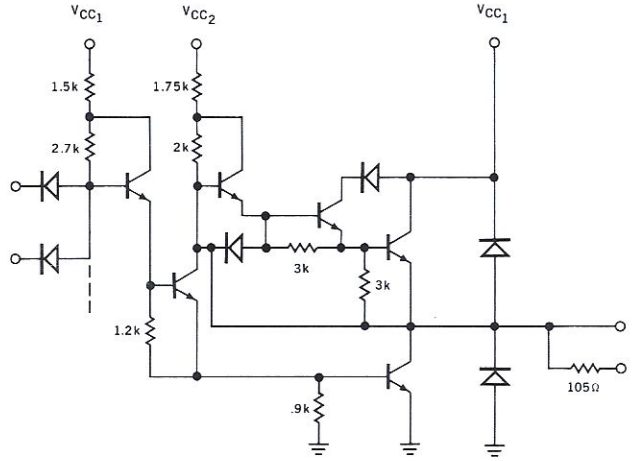


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 linch diameter lead.

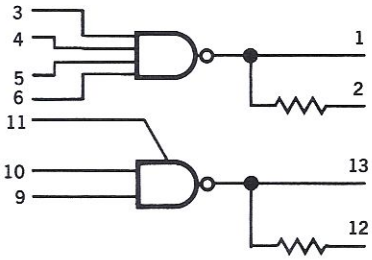
14 PIN FLAT PACKAGE



SCHEMATIC DIAGRAM



LOGIC DIAGRAM



V_{CC_1}=14
V_{CC_2}=8
GND=7

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE −55°C to +125°C (UXX962151X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			−55°C		+25°C			+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		350		200	350		400	mV	$I_{OL} = 20$ mA	$V_{CC1} = 4.5$ V $V_{CC2} = 10.8$ V
V_{OH}		Output High Voltage	4.0		4.0	4.3		4.0		V	$I_{OH} = -20$ mA	$V_{CC1} = 4.5$ V $V_{CC2} = 10.8$ V
I_{SC}	1	Output "Short Circuit" Current			−180	−300				mA	$V_{OUT} = 0$ V	$V_{CC1} = 4.5$ V $V_{CC2} = 10.8$ V
I_{OL}	1	Output Low Current			150	200				mA	$V_{OUT} = 5.0$ V	$V_{CC1} = 4.5$ V $V_{CC2} = 10.8$ V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	$V_F = 0$ V	$V_{CC1} = 5.5$ V $V_{CC2} = 13.2$ V
I_R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	$V_R = 5.5$ V	$V_{CC1} = 5.5$ V $V_{CC2} = 13.2$ V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	$I_{OL} = 2.8$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	$I_{OH} = -2.3$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	$I_{OL} = -20$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	$I_{OH} = 20$ mA	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	$V_{CC1} = 5.5$ V $V_{CC2} = 13.2$ V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	150			ns	$C_L = 5000$ pF	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
t_{pd-}	4	Turn-On Time				80	150			ns		
t_{pd+}		Turn-Off Time				13	25			ns	$C_L = 30$ pF	$V_{CC1} = 5.0$ V $V_{CC2} = 12.0$ V
t_{pd-}		Turn-On Time				9	25			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	$V_{CC1} = 5.5$ V $V_{CC2} = 10.8$ V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	$V_{CC1} = 4.5$ V $V_{CC2} = 13.2$ V	

NOTES:

(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) With both sides loaded at $T_A = +125$°C, maximum frequency = 500 kHz for Dual In-Line package ($\theta_{JA} = 95$°C/W) or 300 kHz for Ceramic Flat Pak ($\theta_{JA} = 165$°C/W).

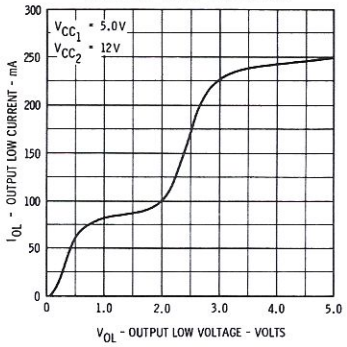
ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE 0°C to +75°C (UXX962159X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		400		200	400		450	mV	I_{OL} = 20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
V_{OH}		Output High Voltage	4.2		4.2	4.4		4.2		V	I_{OH} = −20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{SC}	1	Output "Short Circuit" Current			−100	−300				mA	V_{OUT} = 0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{OL}	1	Output Low Current			75	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V_R = 5.5 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	200			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	200			ns		
t_{pd+}		Turn-Off Time				13	40			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	40			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V	

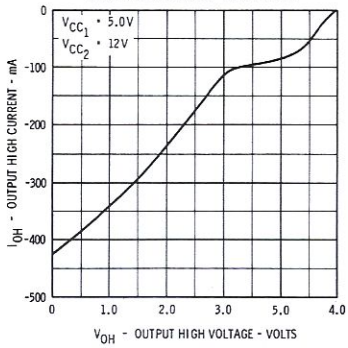
NOTES:

(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C for both Dual In-Line package and Ceramic Flat Pak.

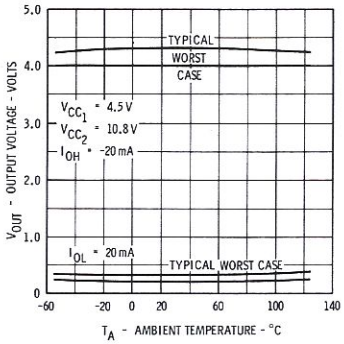
TYPICAL OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



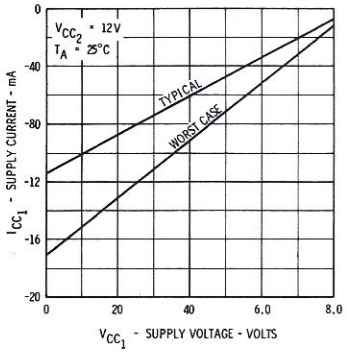
TYPICAL OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



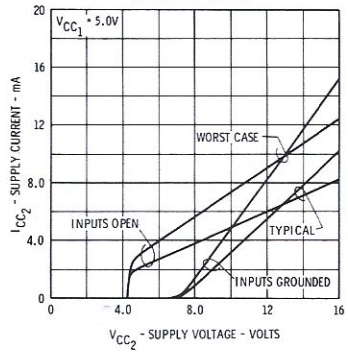
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



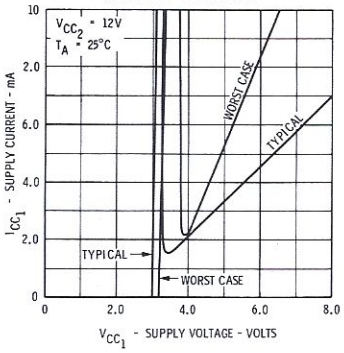
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS GROUNDED



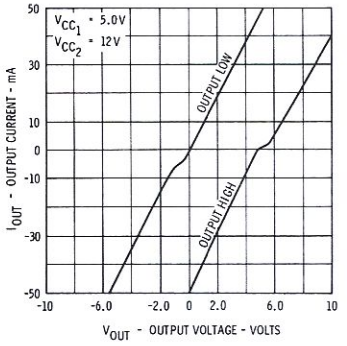
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS OPEN



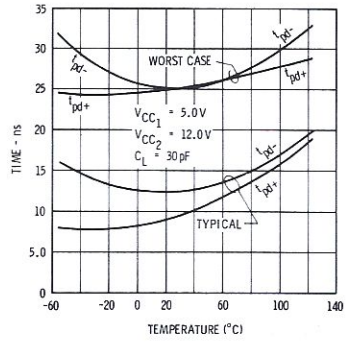
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



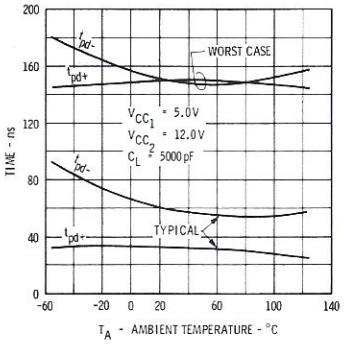
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



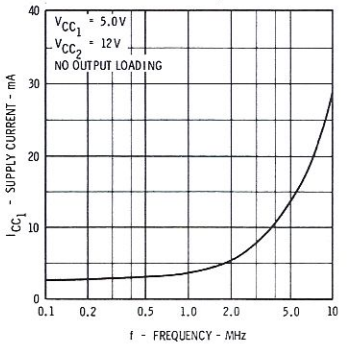
SWITCHING TIME VERSUS TEMPERATURE



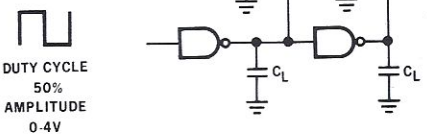
SWITCHING TIME VERSUS TEMPERATURE



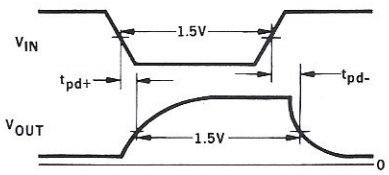
TYPICAL SUPPLY CURRENT VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the "high state" and the "low state" on an I - V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two DC operating points.
3. Choose to analyze either the reflections for the output going low or high. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100\Omega$ in the example), from the "high state" operating point (labeled A on our graph) to the "low state" output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

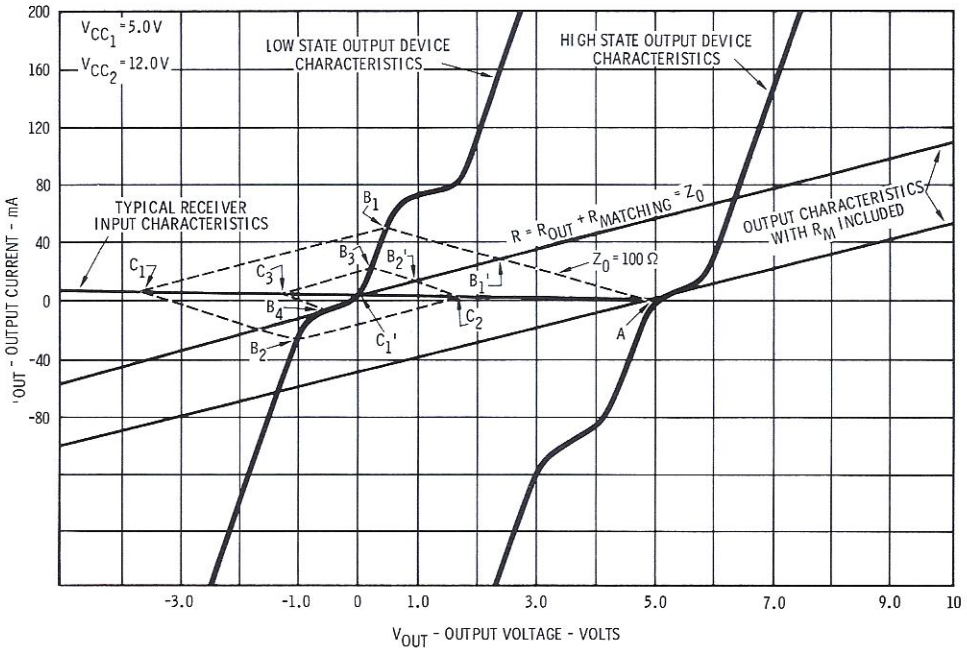
The same procedure is used to check the reflections when switching the output high.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the DC line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the "low state" operating point to B_1.
2. Subtract R_{out} from Z. ($R_{out} + R_M = Z_0$). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1' and C_1' and the receiver will not see any reflections.

When switching the line differentially $R_M + R_{out} = Z_0/2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

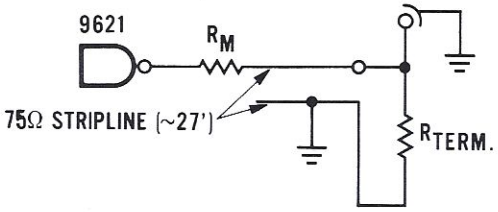
TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

FAIRCHILD INTEGRATED CIRCUIT 9621

REFLECTION TEST CIRCUIT

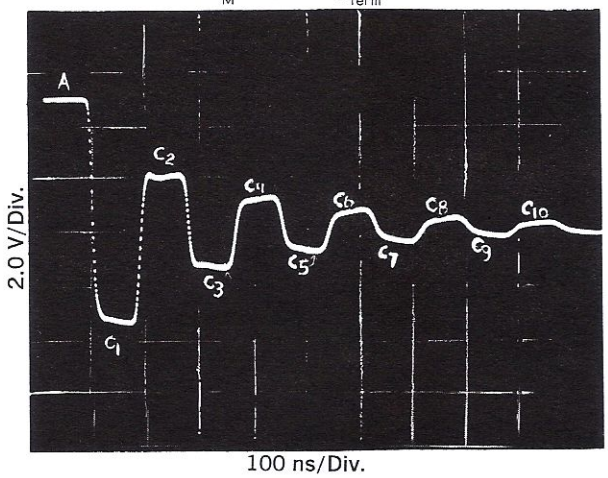


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

BACK MATCHING TABLE

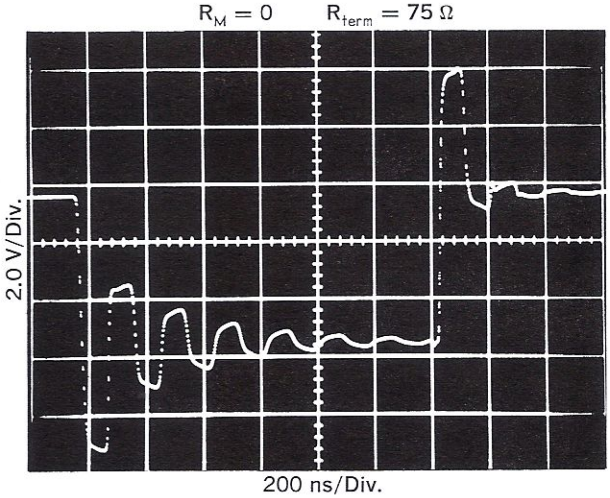
Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

$R_M = 0$ $R_{term} = \infty$



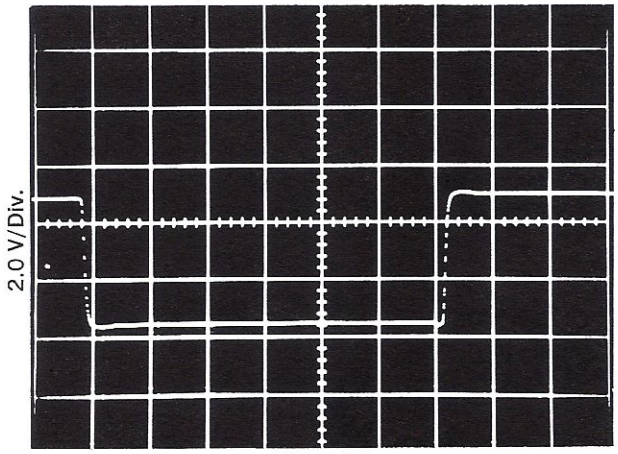
100 ns/Div.

$R_M = 0$ $R_{term} = 75\ \Omega$



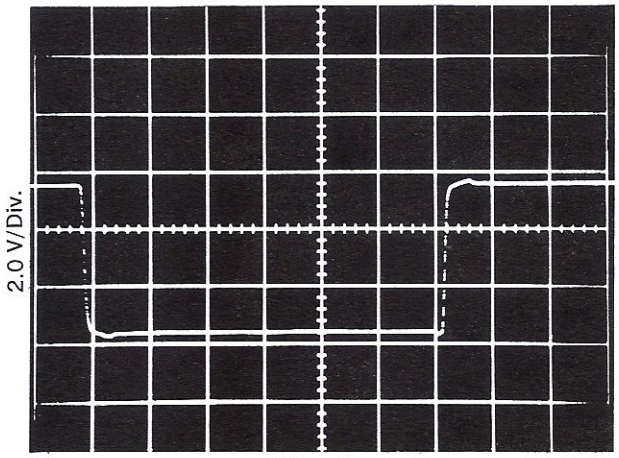
200 ns/Div.

$R_M = 0$ $R_{term} = 75\Omega$



200 ns/Div.

$R_M = 62\ \Omega$ $R_{term} = \infty$



200 ns/Div.

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